

T36014

100

144

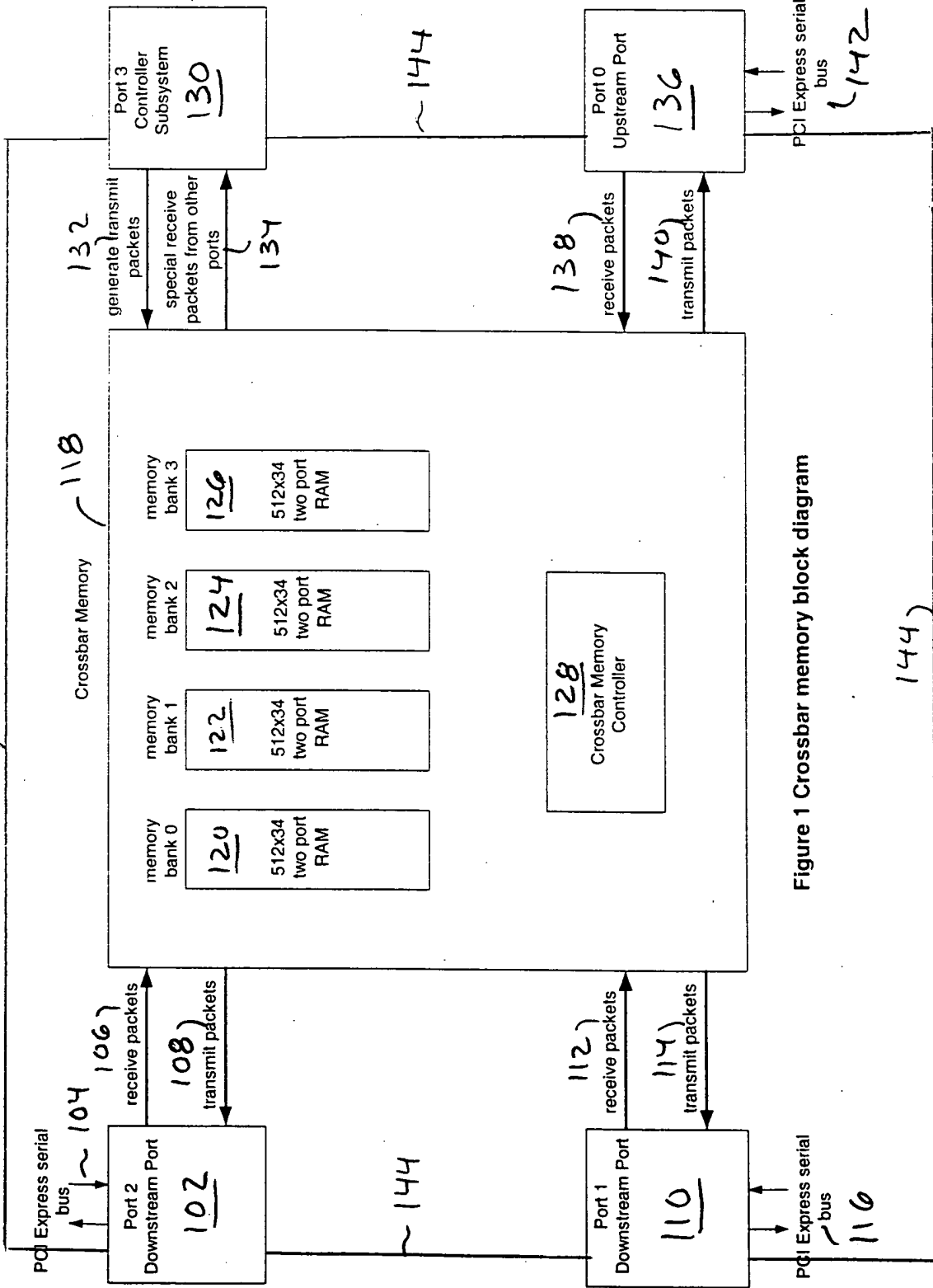


Figure 1 Crossbar memory block diagram

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200)

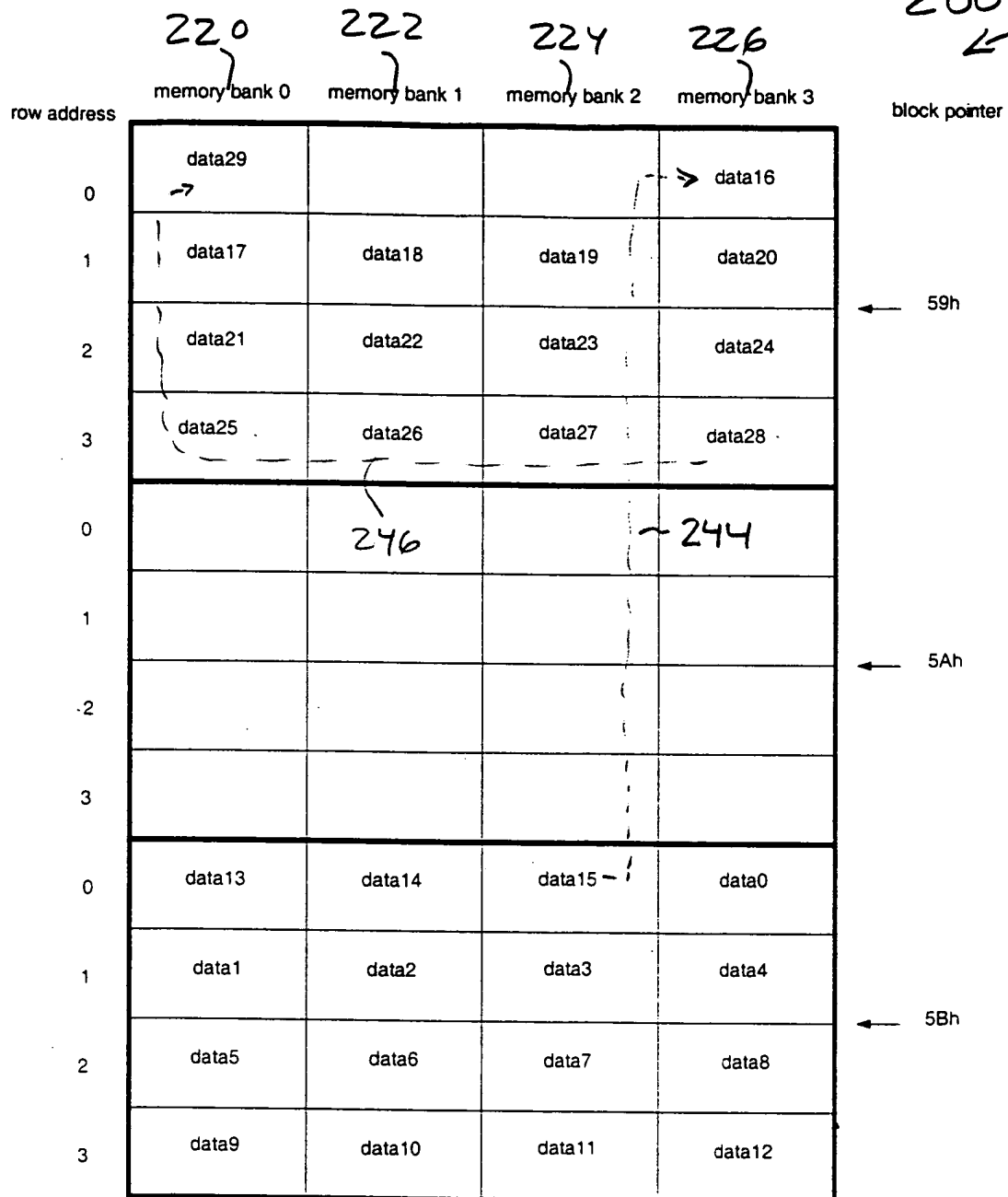


Figure 2 Crossbar memory packet storage

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300)

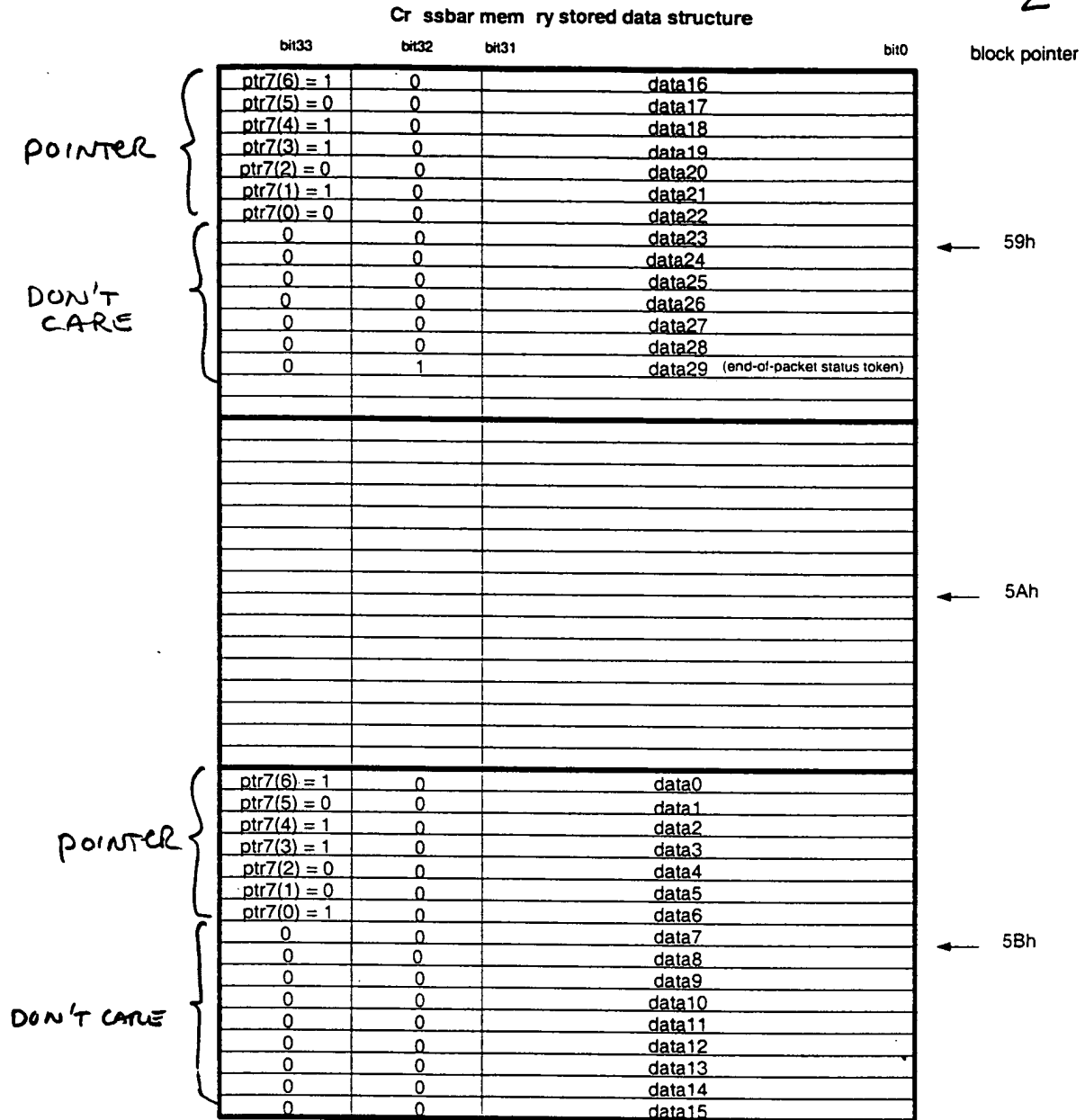


Figure 3 PCI Express packet storage data structure

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400

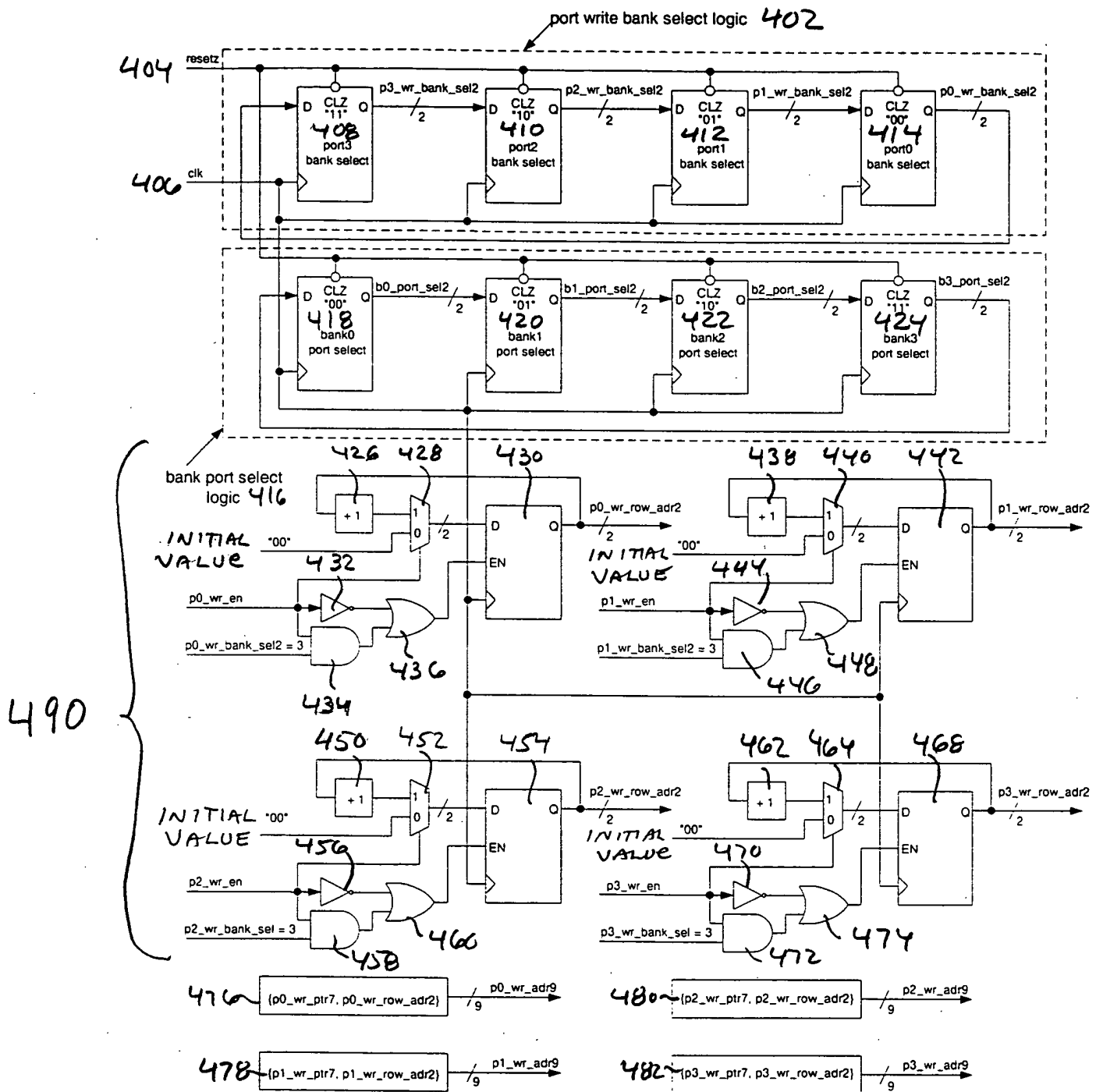


Figure 4 Crossbar memory controller - bank select, port select and write address logic

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500

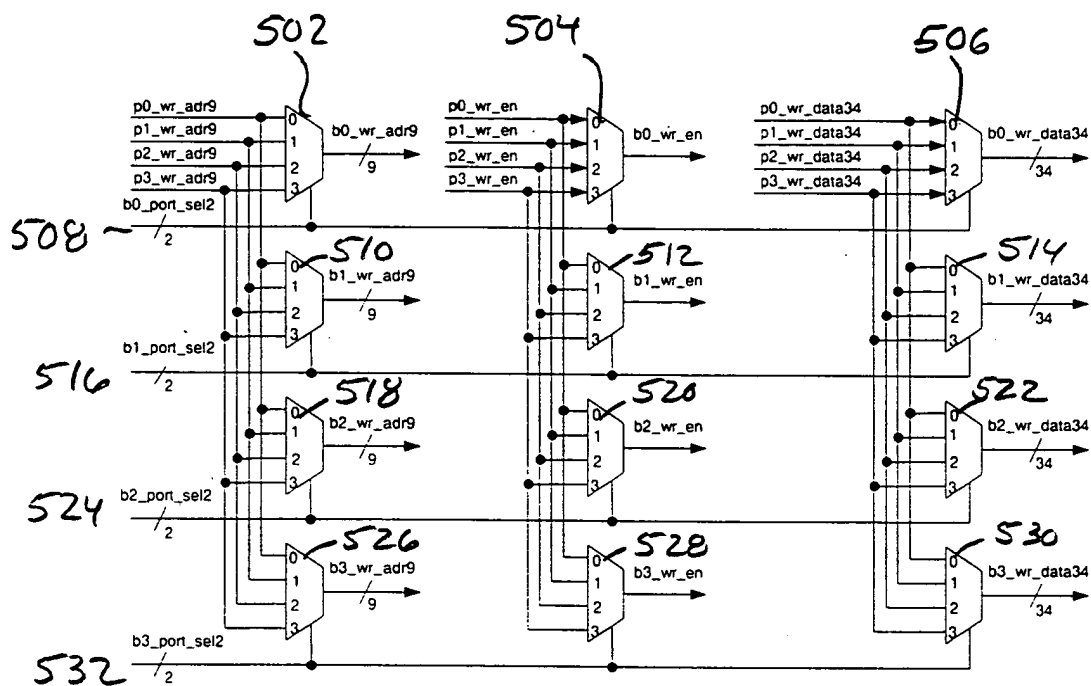


Figure 5 Crossbar memory controller - memory bank write mutiplex logic

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600

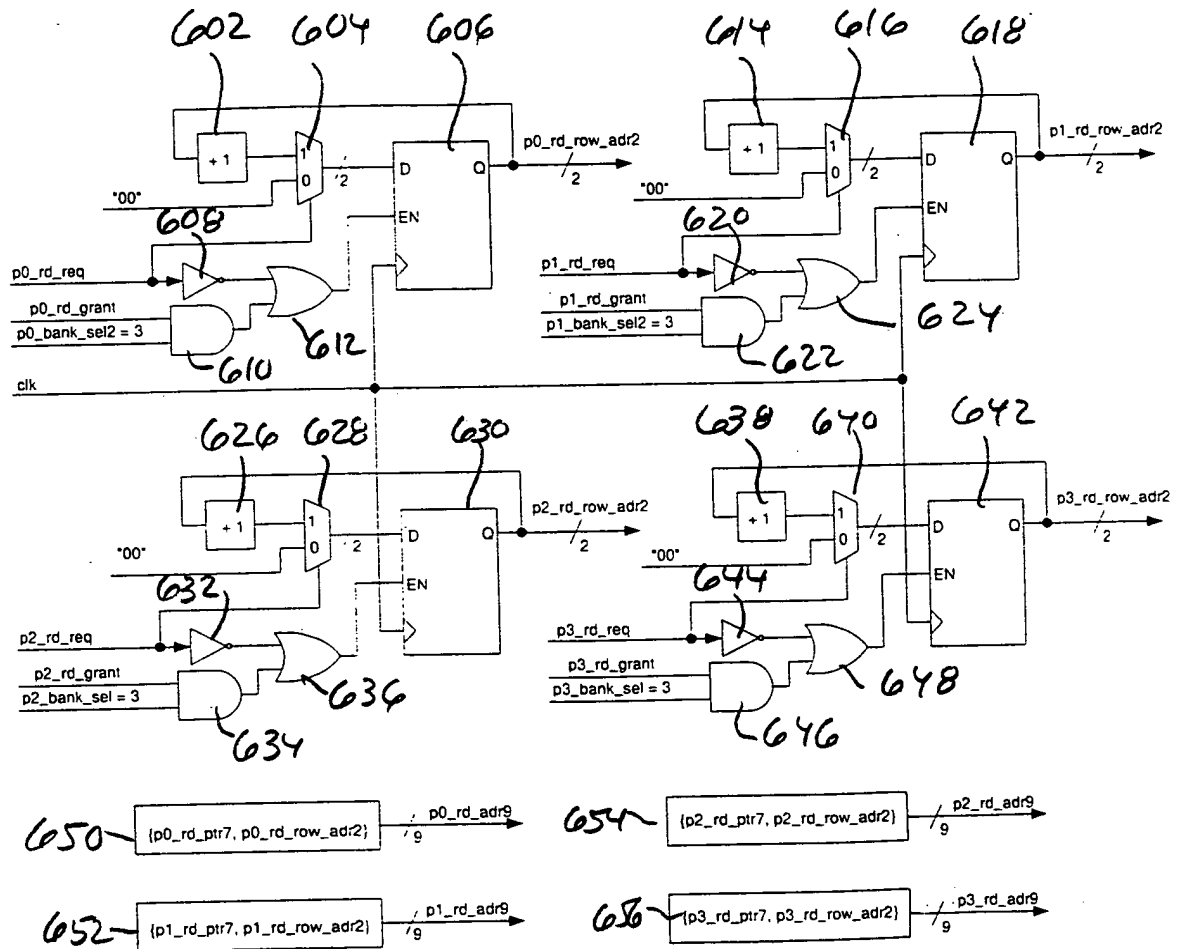


Figure 6 Crossbar memory controller - port read address logic

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700

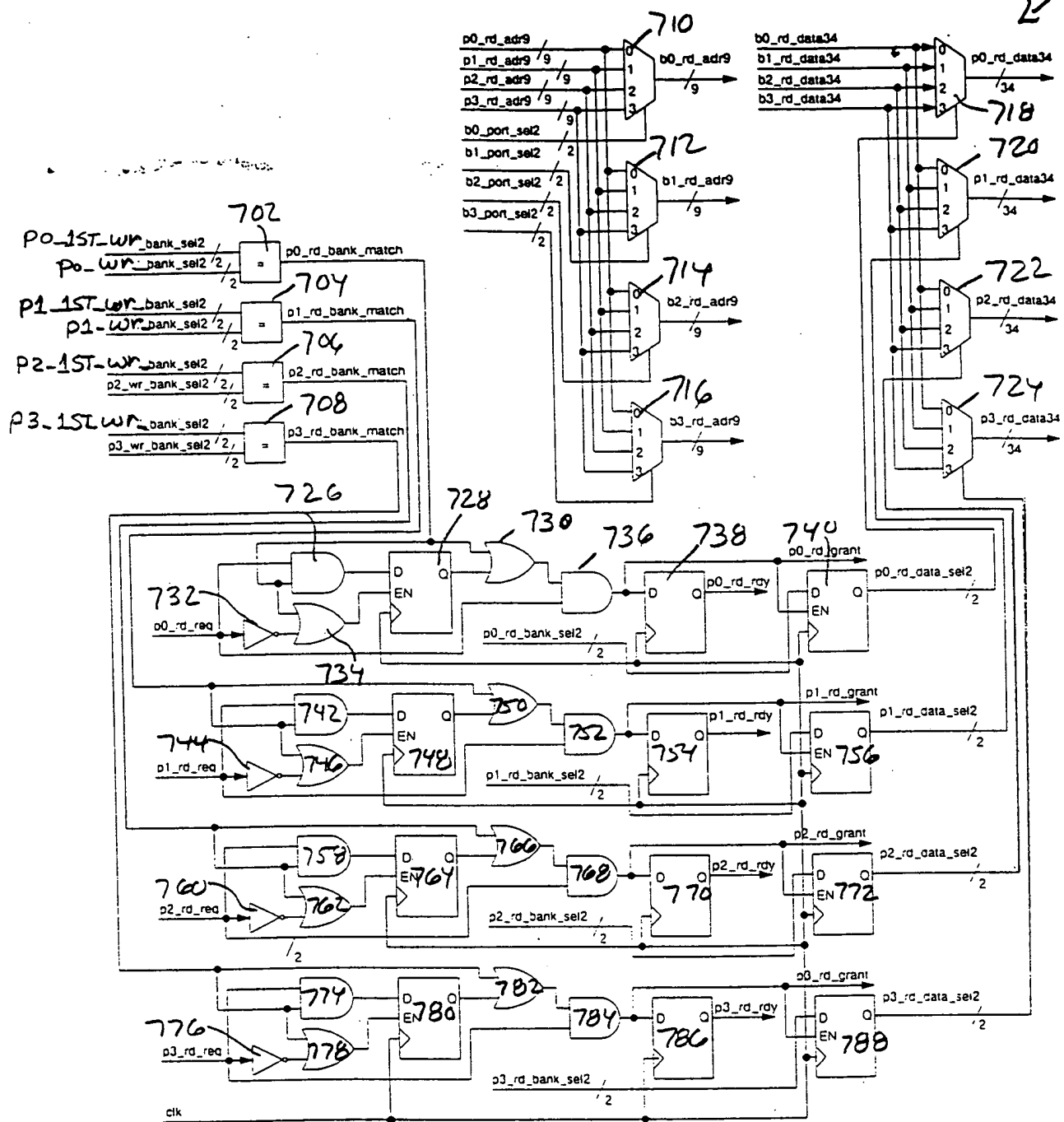


Figure 7 Crossbar memory controller - memory bank read control logic

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800
↙

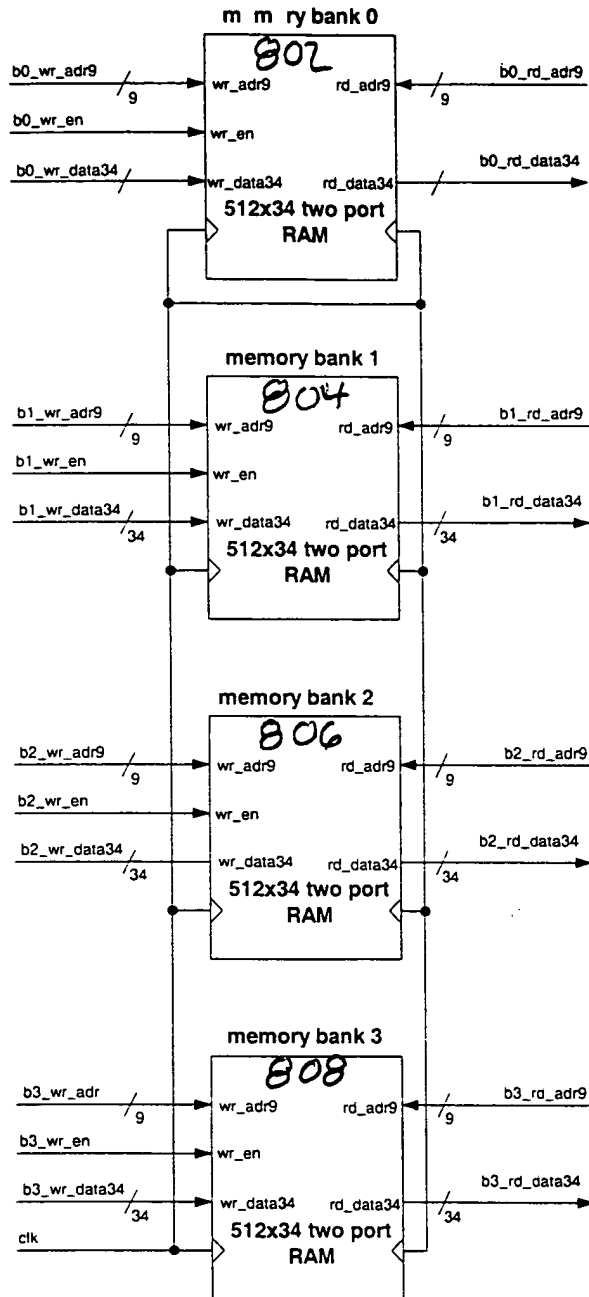
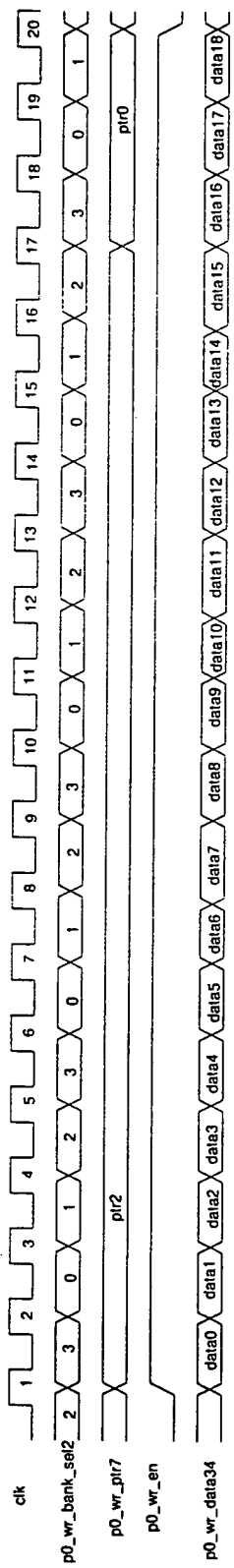


Figure 8 Crossbar memory bank access interface signals

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900
2



Note: In this example port 0 start writing crossbar memory from memory bank 3

Figure 9 port receive packet write timing diagram

clk	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
p2_wr_bank_sel2	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0
p2_wr_bank_sel2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2
p2_rd_ptr7	ptr0																			
p2_rd_ptr7	ptr2																			
p2_rd_req																				
p2_rd_grant																				
p2_rd_rdy																				
p2_rd_data34	data0	data1	data2	data3	data4	data5	data6	data7	data8	data9	data10	data11	data12	data13	data14	data15	data16	data17	data18	data19
don't care																				

Figure 10 port transmit packet read timing diagram -1

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1100
2

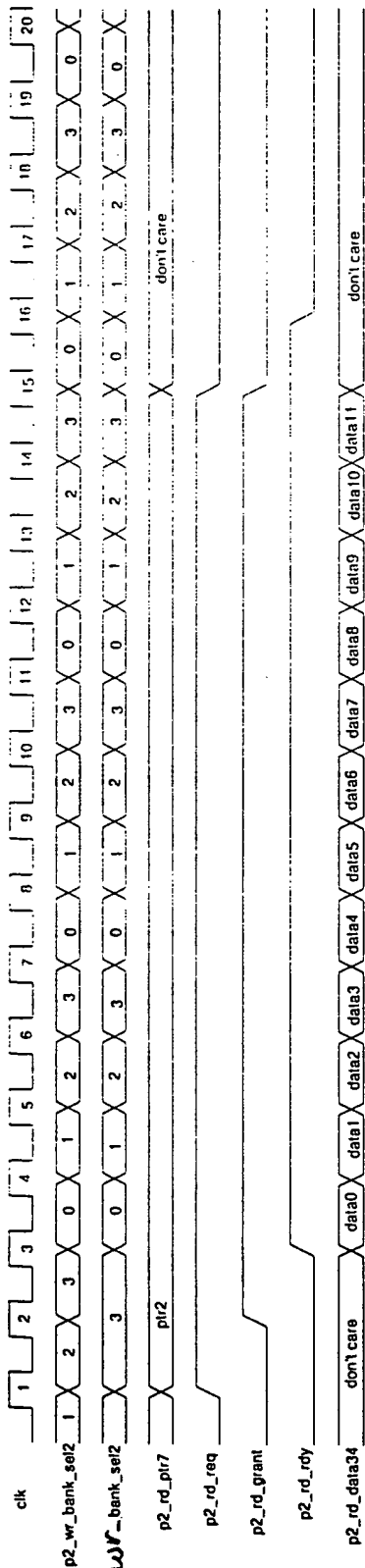


Figure 11 port transmit packet read timing diagram -2 (shown read termination)

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1200

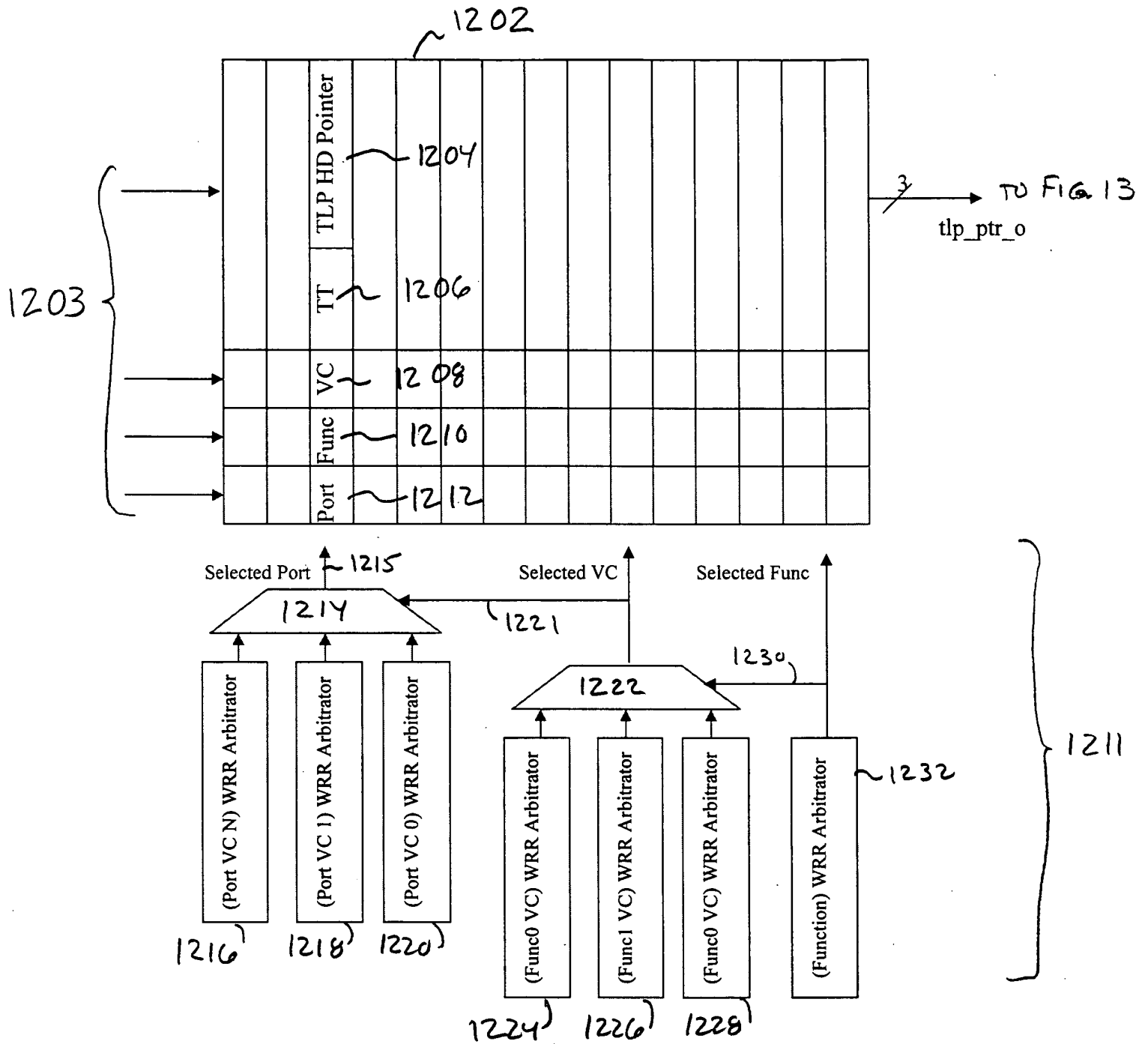


FIG. 12

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1300

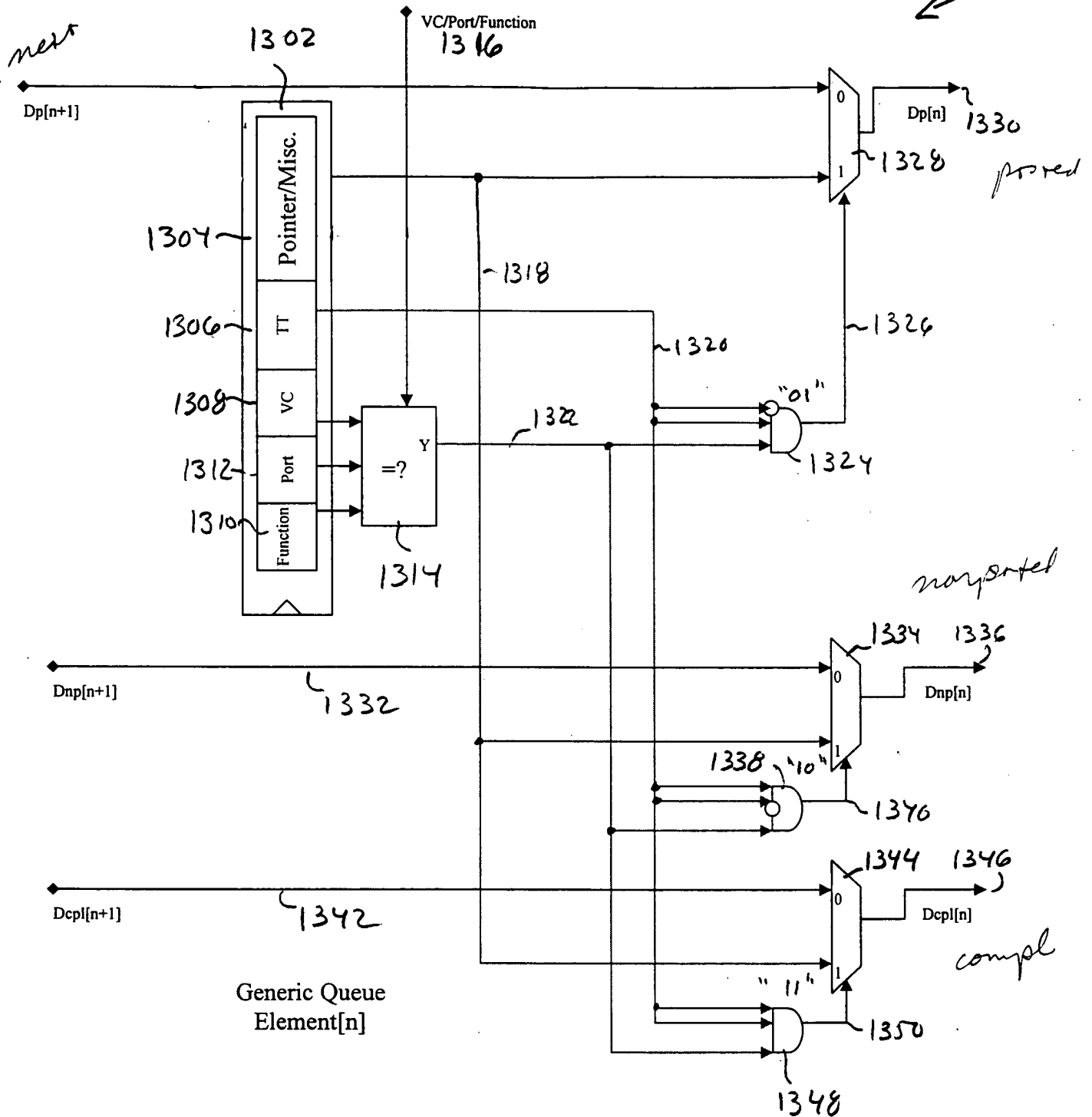


FIG. 13